Claims

1. A ferroelectric memory transistor comprising:
a silicon substrate having a drain region and a source region; and
a stacked gate structure including:
a first insulative layer on the silicon substrate between the drain and source regions;
a ferroelectric layer; and
a doped insulative layer between the first insulative layer and the ferroelectric layer.

2. The transistor of claim 1, wherein the ferroelectric layer is a weak ferroelectric layer.

3. The transistor of claim 1, wherein the ferroelectric layer has a dielectric constant less than 1000.

4. The transistor of claim 1, wherein the ferroelectric layer is characterized by a spontaneous polarization within a range of approximately 0.01 micro-Coulomb/cm^2 to 1 micro-Coulomb/cm^2.

5. The transistor of claim 1, wherein the doped insulative layer has a dielectric constant between that of the first insulative layer and that of the ferroelectric layer.

6. The transistor of claim 1, wherein the first insulative layer has a dielectric constant of about 4, the doped insulative layer has a dielectric constant of about 165 or 180, and the ferroelectric layer has a dielectric constant of about 250.

7. The transistor of claim 1, wherein the first insulative layer consists essentially of a silicon oxide.

8. The transistor of claim 1, wherein the doped insulative layer comprises at least one of strontium- or barium-doped titanium oxide.

9. The transistor of claim 1, wherein the ferroelectric layer consists essentially of zinc oxide doped with lithium at a level of about 1 mol percent to about 30 mol percent of the metal component.

10. The transistor of claim 1, wherein the ferroelectric layer consists essentially of zinc oxide doped with magnesium at a level of about 1 mol percent to about 30 mol percent of the metal component.

11. A ferroelectric memory transistor comprising:

a silicon substrate having a drain region and a source region; and

a stacked gate structure including:

a first insulative layer on the silicon substrate between the drain and source regions;

a ferroelectric layer characterized by a spontaneous polarization in a range of approximately 0.01 micro-Coulomb/cm^2 to 1 micro-Coulomb/cm^2; and

a doped insulative layer between the first insulative layer and the weak ferroelectric layer.

12. A ferroelectric memory transistor comprising:

a silicon substrate having a drain region and a source region; and

a stacked gate structure including:

a first insulative layer on the silicon substrate between the drain and source regions;

a ferroelectric layer characterized by a spontaneous polarization in a range of approximately 0.01 micro-Coulomb/cm^2 to 1 micro-Coulomb/cm^2; and

a doped insulative layer between the first insulative layer and the ferroelectric layer, the doped insulative layer having a dielectric constant between that of the first insulative layer and that of the ferroelectric layer.

13. A ferroelectric memory transistor comprising:
a silicon substrate having a desired channel conduction region;
a silicon-oxide layer over the desired channel conduction region;
a strontium-doped titanium-oxide layer on the silicon-oxide layer;
a doped zinc-oxide layer on the doped titanium-oxide layer;
a gate conductor on the zinc-oxide layer

14. A ferroelectric memory transistor comprising:
a silicon substrate having a desired channel conduction region;
a silicon-oxide layer over the desired channel conduction region;
a strontium-doped titanium-oxide layer on the silicon-oxide layer;
a lithium-doped zinc-oxide layer on the doped titanium-oxide layer;
a gate conductor on the lithium-doped zinc-oxide layer.

15. A ferroelectric memory transistor comprising:
a silicon substrate having a desired channel conduction region;
a silicon-oxide layer over the desired channel conduction region;
a strontium-doped titanium-oxide layer on the silicon-oxide layer;
a magnesium-doped zinc-oxide layer on the doped titanium-oxide layer;
a gate conductor on the magnesium-doped zinc-oxide layer.

16. A ferroelectric memory transistor comprising:

a silicon substrate having a desired channel conduction region;

a silicon-oxide layer over the desired channel conduction region;

a barium-doped titanium-oxide layer on the silicon-oxide layer;

a doped zinc-oxide layer on the barium-doped titanium-oxide layer; and

a gate conductor on the zinc-oxide layer.

17. A method for making a ferroelectric memory transistor, the method comprising:

forming a silicon-oxide layer over a desired channel region of a silicon substrate;

wherein forming the silicon-oxide layer comprises:

establishing a chamber temperature of approximately 400 degrees Celsius;

generating oxygen atoms in a Krypton plasma;

forming a doped titanium-oxide layer over the silicon-oxide layer; and

forming a doped zinc-oxide layer on the titanium-oxide layer.

18. The method of claim 17 wherein forming the doped titanium-oxide layer over the silicon-oxide layer comprises:

using atomic-layer deposition to form a strontium- or barium-doped titanium-oxide layer.

19. The method of claim 17 wherein forming the doped titanium-oxide layer over the silicon-oxide layer comprises:

using atomic-layer deposition to form a strontium- or barium-titanate layer.

20. The method of claim 18, wherein using atomic-layer deposition comprises:

establishing an ambient pressure of about 10 mbar within a deposition chamber containing the silicon-oxide layer;

establishing an ambient temperature between 250 and 325 degrees Celsius within the deposition chamber;

alternately introducing a strontium or barium precursor and a titanium-oxide precursor into the deposition chamber, with the strontium or barium precursor and the titanium-oxide precursors introduced at rates to saturate reactions of the precursors at a surface of the silicon-oxide layer; and

introducing water vapor into the deposition chamber concurrent with the introduction of the strontium or barium precursor and concurrent with the introduction of the titanium-oxide precursors.

21. The method of claim 19, wherein the strontium or barium precursors consists essentially of cyclopentadienyl compounds.

22. The method of claim 19, wherein the strontium or barium precursors consists essentially of $Sr(C_5\text{-I-}Pr_3H_2)_2$ or $Ba(C_5Me_5)_2$.

23. The method of claim 20, further comprising:

purging the deposition chamber with nitrogen gas between alternate introductions of the strontium or barium precursors and the titanium-oxide precursors.

24. The method of claim 17 wherein forming the doped zinc-oxide layer comprises:

providing a composite mass comprising zinc oxide and particles of lithium or magnesium; and

magnetron sputtering matter from the composite mass onto the titanium-oxide layer.

25. The method of claim 17 wherein forming the doped zinc-oxide layer comprises:

jet-vapor deposition of zinc oxide, (lithium carbonate), and magnesium oxide on the titanium-oxide layer.

26. The method of claim 17 wherein forming the doped zinc-oxide layer comprises:

chemical-vapor deposition of zinc-oxide on the titanium-oxide layer.

27. A method for making a ferroelectric memory transistor, the method comprising:

forming a silicon-oxide layer over a desired channel region of a silicon substrate;

forming a doped titanium-oxide layer over the silicon-oxide layer, wherein forming the doped titanium-oxide layer comprises

establishing an ambient pressure of about 10 mbar within a deposition chamber containing the silicon-oxide layer;

establishing an ambient temperature between 250 and 325 degrees Celsius within the deposition chamber;

alternately introducing a dopant precursor and a titanium-oxide precursor into the deposition chamber; and

introducing water vapor into the deposition chamber concurrent with the introduction of the strontium or barium precursor and concurrent with the introduction of the titanium-oxide precursors; and

forming a doped zinc-oxide layer on the doped titanium-oxide layer.

28. The method of claim 27 wherein the dopant precursor includes strontium or barium.

29. A method for making a ferroelectric memory transistor, the method comprising:

forming a silicon-oxide layer over a desired channel region of a silicon substrate;

forming a doped titanium-oxide layer over the silicon-oxide layer; and

forming a doped zinc-oxide layer on the titanium-oxide layer, wherein forming the doped zinc-oxide layer comprises:

providing a composite mass comprising zinc oxide and particles of lithium or magnesium; and

magnetron sputtering matter from the composite mass onto the titanium-oxide layer.

30. A method for making a ferroelectric memory transistor, the method comprising:

forming a silicon-oxide layer over a desired channel region of a silicon substrate;

forming a doped titanium-oxide layer over the silicon-oxide layer; and

forming a doped zinc-oxide layer on the titanium-oxide layer, wherein forming the doped zinc-oxide layer comprises:

jet-vapor deposition of zinc oxide in combination with lithium carbonate or magnesium oxide on the titanium-oxide layer.

31. A method for making a ferroelectric memory transistor, the method comprising:

forming a silicon-oxide layer over a desired channel region of a silicon substrate, wherein forming the silicon-oxide layer comprises:

establishing a chamber temperature of approximately 400 degrees Celsius;

generating oxygen atoms in a Krypton plasma;

forming a doped titanium-oxide layer over the silicon-oxide layer, wherein forming the doped titanium-oxide layer comprises:

establishing an ambient pressure of about 10 mbar within a deposition chamber containing the silicon-oxide layer;

establishing an ambient temperature between 250 and 325 degrees Celsius within the deposition chamber;

alternately introducing a dopant precursor and a titanium-oxide precursor into the deposition chamber; and

introducing water vapor into the deposition chamber concurrent with the introduction of the strontium or barium precursor and concurrent with the introduction of the titanium-oxide precursors; and

forming a doped zinc-oxide layer on the titanium-oxide layer, wherein forming the doped zinc-oxide layer comprises:

providing a composite mass comprising zinc oxide and particles of lithium or magnesium; and

magnetron sputtering matter from the composite mass onto the titanium-oxide layer.

32. A system comprising:

at least one processor; and

a memory device coupled to the one processor, wherein the memory device comprises a plurality of ferroelectric memory transistors, with each transistor comprising:

a silicon substrate having a drain region and a source region; and

a stacked gate structure including:

a first insulative layer on the silicon substrate between the drain and source regions;

a ferroelectric layer; and

a doped insulative layer between the first insulative layer and the ferroelectric layer.

33. The system of claim 32, wherein the ferroelectric layer has a dielectric constant less than 1000.

34. The system of claim 33, wherein the ferroelectric layer is characterized by a spontaneous polarization in a range of approximately 0.01 micro-Coulomb/cm^2 to 1 micro-Coulomb/cm^2.

35. The system of claim 33, wherein the doped insulative layer has a dielectric constant between that of the first insulative layer and that of the ferroelectric layer.

36. The system of claim 33, wherein the first insulative layer consists essentially of a silicon oxide.

37. The system of claim 33, wherein the doped insulative layer comprises at least one of strontium- or barium-doped titanium oxide.

38. The system of claim 33, wherein the ferroelectric layer consists essentially of zinc oxide doped with magnesium at a level of about 1 mol percent to about 30 mol percent of the metal component.

39. A system comprising:

at least one processor; and

a memory device coupled to the one processor, wherein the memory device comprises a plurality of ferroelectric memory transistors, with each transistor comprising:

a silicon substrate having a drain region and a source region; and

a stacked gate structure including:

a first insulative layer on the silicon substrate between the drain and source regions;

a ferroelectric layer characterized by a spontaneous polarization within a range of approximately 0.01 micro-Coulomb/cm^2 to 1 micro-Coulomb/cm^2; and

a doped insulative layer between the first insulative layer and the ferroelectric layer.

40. The system of claim 39, wherein the doped insulative layer has a dielectric constant between that of the first insulative layer and that of the ferroelectric layer.

41. The system of claim 39, wherein the first insulative layer consists essentially of a silicon oxide.

42. The system of claim 39, wherein the doped insulative layer comprises at least one of strontium- or barium-doped titanium oxide.